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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/558,718	11/29/2005	Adrainus Bernardus Smolders	NL 030684	7071

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NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
KINKEAD, ARNOLD M	
ART UNIT	**PAPER NUMBER**
2817	

NOTIFICATION DATE	DELIVERY MODE
02/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/558,718	SMOLDERS ET AL.	
	Examiner	Art Unit	
	Arnold Kinkead	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,6 and 8* is/are rejected.

7)☒ Claim(s) *2,4,7,9-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1,3,5,6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cabral, Jr. et al(US 6,700,203) in view of Grivna et al(US 6,984,860).

The reference by Cabral, Jr. et al discloses an electronic device that includes a resistive layer formed on top of the capacitive trenches, see figure 5, and col.4, top paragraph.

"(22) The present invention is still further directed to an electronic structure that has an in-situ formed unit resistor in electrical communication with a capacitor which includes a unit resistor that is formed by a first conductive element and a second conductive element situated in different levels in the

electronic structure connected therein between by an electrically resistive via, the electrically resistive via may be formed of a material that has a resistivity of at least 100 .OMEGA.-cm; and a capacitor formed juxtaposed to and in electrical communication with the unit resistor.

(23) In the electronic structure that has an in-situ formed unit resistor in electrical communication with a capacitor, the capacitor may be a deep-trench capacitor or a stacked capacitor. The unit resistor may be electrically connected in-series with the capacitor, or electrically connected in-parallel with the capacitor. The unit resistor may be electrically connected to and situated on top of the capacitor, or electrically connected to and situated below the capacitor. The electrically resistive via may be formed of a refractory metal-silicon-nitrogen...

See col. 9, lines 13-20:

"For certain application, RC components are used to build filter, heater, delay chain, etc. Or they can also be used as elements for an analog circuit application. "

As described above the resistor and capacitor arrangement can be used in filter arrangements, for example, an LPF filter(see Grivna et al below) in a PLL circuit. Official notice is taken with respect to a LPF for a PLL with phase detection, charge pump and VCO. Also, the particular values of the trench capacitors would be part of such an implementation for achieving the proper control voltage.

Figure 5, shows resistors (82) and parallel capacitors coupled to ground.

The reference by Cabral, Jr. et al does not explicitly describe the dielectric film(Silicon Nitride) layer forming the capacitor, nor the use of such a combination of elements as a low pass filter. The reference does not describe a combination of small and large capacitance trenches. There is suggestion, however, for such a configuration, see col. 9, lines 5-16 for sizing the capacitor as desired.

The reference does not explicitly describe the polysilicon layer for the resistor where the upper portion of the caps are defined as well as the stacking construct.

The reference by Grivna et al from the same field of endeavor is relied on to show some of these ideas, for example, with regards the use of the filter as a low pass filter, see background of invention, second para. With regards the Silicon Nitride layer,

See col. 3, lines 27-40(ref '860):

"A dielectric film 33 is formed over outer surface 32 to function as a capacitor dielectric. Dielectric film 33 is grown or deposited using a conformal process that results in a constant thickness over all of the underlying topographies of semiconductor device 10. The constant thickness of dielectric film 33 is facilitated by the conformal nature of conductive layer 22, whose outer surface 32 is smoother than the contours underlying its inner surface. In one embodiment, dielectric film 33 comprises **silicon nitride** deposited to a thickness in a range

between about forty and about six hundred angstroms, with a typical thickness of about four hundred angstroms."

With regards the use of polysilicon layer for the resistors, near the upper portions of the capacitor trenches, see col. 4, top paragraph:

"(24) A conductive film 36 is disposed over dielectric film 33 and then patterned and etched to form plates 38 that contact exposed portions of conductive layer 35 near the openings of trenches 18 as shown. In one embodiment, plates 38 are formed with undoped polycrystalline silicon deposited to a thickness of about one thousand eight hundred angstroms and then patterned and doped to have a p-type conductivity suitable for forming resistors,..."

Also, suggestion for the stacking implementation is in col. 3, lines 39-42, where a stack implementation (stack die) is described:

"In an alternative embodiment, dielectric film 33 is formed as a dielectric stack consisting of, for example, an oxide-nitride stack or an oxide-nitride-oxide stack."

Again, the use of an LPF in analog PLL's is conventional and allows for the development of the control signal to the VCO as is notoriously well known in the art.

In light of the above it would have been obvious to one of ordinary skill in the art to have recognized that the general filter arrangement of Cabral, Jr. et al could be part of a low pass filter arrangement, with the integrated construct as described

above in Grivna et al to allow for a more integrated and compact electronic application with resistors and trench capacitors together. The particular capacitor values(large/small) being part of the PLL design as noted above.

Allowable Subject Matter

Claims 2,4,7, 9-11 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 11-21-07 have been fully considered but they are not persuasive. The examiner maintains the rejection in light of applicants' remarks regarding that no suggestion exists in the applied primary reference for the size of the capacitors used...however, as is suggested in col. 9, lines 6-16, of the **reference by Cabral, Jr. et al., use of any sized caps(in parallel) may be determined by any desirable number of deep trench capacitors and thus small and large type caps may be configured this way.**

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arnold Kinkead whose telephone number is 571-272-1763. The examiner can normally be reached on Hoteling.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arnold Kinkead
/Arnold Kinkead/

Primary Examiner, Art Unit 2817